

## Guest Editorial

**M**OVING into the 21st century, the semiconductor industry faces new challenges in the manufacturing of deep sub-quarter micron devices. These challenges include invention of innovative processes, development of effective process control techniques, and management of the change from vertically integrated fabs to foundries. Some of these issues were addressed in the 88 high quality papers presented at the 8th Annual Advanced Semiconductor Manufacturing Conference and Workshop (ASMC), held in Boston, MA, September 10-12, 1997. This annual forum provides a venue for the presentation of experience, methodologies, approaches, and techniques that are required to achieve and maintain world class semiconductor manufacturing status.

This special issue of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING comprises of five selected papers from ASMC'97. The papers present tools and approaches that contribute to manufacturing excellence. With the advent of automatic defect classification, better process control techniques are necessary to factor in the information generated by sophisticated inspection and monitoring of processes. The paper by Shindo *et al.* describes how the effectiveness of process control can be improved by using defect classification data. Shindo *et al.* propose a novel defect grouping scheme and analytical models that are useful for detecting critical killer defect excursions.

Yield improvement using experimental work will become expensive with the advent of 300 mm wafers. The paper by Milor *et al.* explains how prohibitive experimental costs can be avoided by using efficient simulation methods for process diagnosis. The application of this technique is in its infancy, but is expected to eventually play a key role in improving yield. With advanced inspection technology, it is now possible to estimate the distribution of defect sizes and shapes, which

are critical inputs for evaluating the defect limited yield. The paper by Milor provides a methodology for yield estimation that incorporates the distribution of defects as well as the error in size estimation.

The paper by Singh *et al.* describes rapid photo-thermal process. Singh *et al.* suggest that certain defects are not large enough to be detected as morphological faults. Such defects can be estimated by using the total value of stress of the material. The new process is aimed toward stress reduction. The authors motivate the need for process optimization, provide a step-by-step methodology for determining the process parameters, and describe experimental results.

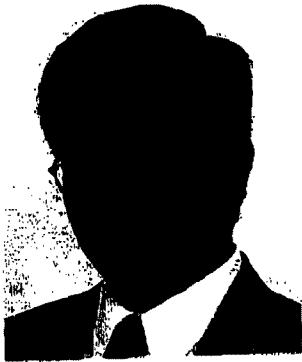
The business in the semiconductor industry is moving from vertically integrated models to fabless-foundry models. The paper by Chatterjee *et al.* provides an analytical framework for studying fabless-foundry partnerships. It addresses the key yield management issues in the burgeoning fabless-foundry sector of the semiconductor industry.

We would like to thank Dave T. Fletcher, General Chair, Scott R. McClure, Conference Chair, and John Goodman, Technical Chair of ASMC'97, for generating the idea about this special issue and providing us with the opportunity to do so. Our sincere thanks go to the Editor, Dr. Gary May, for assisting us with the special issue. We would like to express our thanks to several anonymous referees for providing the reviews on multiple versions of the submitted papers at a short notice. Our special thanks also to Prof. Jayashankar Swaminathan, Haas School of Business, University of California, Berkeley, for acting as an associate editor for some of the papers. We would also like to thank Darlene Bush for taking care of all IEEE related matters and for her help in compiling this special issue.

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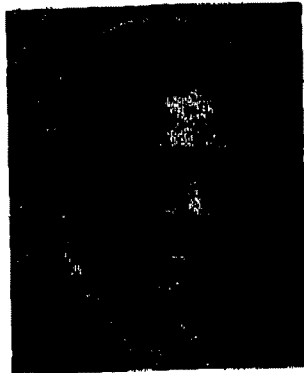


Raman K. Nurani received the B.S. degree in mechanical engineering from the Indian Institute of Technology, Madras, in 1984, the M.B.A. degree from the Loyola Institute of Business Administration, Madras, in 1990, and the M.S. and Ph.D. degrees in management of manufacturing and automation from Carnegie Mellon University, Pittsburgh, PA, in 1992 and 1995, respectively.

He was a Design and Process Engineer and Manufacturing Systems Manager with Sundram Fasteners Ltd, Madras, from 1984 to 1990. He is currently a Senior Research Scientist at KLA-Tencor Corporation, San Jose, CA, where he has been since 1994. During 1993-1994, as a visiting student in the Department of Industrial Engineering and Operations Research at the University of California, Berkeley, he was actively involved in the Sloan Focus study on yield management and the SRC funded project on Production Logistics Techniques Incorporation Yield Analysis. He has interacted with Advanced Micro Devices (AMD), Texas Instruments, Digital, Intel, IBM and Hewlett-Packard to develop, validate, and implement his research work.

He teaches M.B.A. and undergraduate courses part-time in the Leavey School of Business at Santa Clara University, Santa Clara, CA. His current research focuses on the development of models and methodologies in the area of yield management and automated wafer inspection.

Dr. Nurani received the honorable mention in the 1995 George B. Danzig Award from INFORMS, the Institute for Operations Research and Management Science, for the best Ph.D. dissertation that is innovative and relevant to the practice of operations research and management science.



Sridhar Seshadri received the B.Tech. degree from the Indian Institute of Technology, Madras, India, in 1978, the Post Graduate Diploma in management from the Indian Institute of Management, Ahmedabad, India, in 1980, and the Ph.D. degree in management science from the University of California, Berkeley, in 1993.

He has worked as an Engineer in a medium and heavy engineering firm in India, as a Contractor in the Middle East as well as India, and as a Professor for five years in the Operations Management Area, Administrative Staff College, Hyderabad, India. He is currently with the Department of Statistics and Operations Management, Leonard N. Stern School of Business, New York University. His research interests are in the area of stochastic modeling and optimization, with applications to manufacturing, distribution, telecommunications, database design, insurance, and finance.

Dr. Seshadri is an Associate Editor for *Naval Research Logistics and Telecommunications Systems*, and on the Editorial Review Board of *Production and Operations Management*.

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- ⊘ or ⅈ or 7 delete; take ~~x~~ out
- ⊘ close up; print as one word
- ⊘ delete and close up
- ^ or > or ^ caret; insert here *(something)*
- # insert space
- eg# space evenly <sup>^</sup> where indicated
- set let marked ~~text~~ stand as set
- ↔ transpose; change order *(the)*
- / used to separate two or more marks and often as a concluding stroke at the end of an insertion
- [ set farther to the left
- ] set farther to the right
- ^ set ae or fi as ligatures æ or fi
- = straighten alignment
- || || straighten or align
- x imperfect or broken character
- indent or insert em quad space
- ¶ begin a new paragraph
- Ⓟ spell out (set 5 lbs) as five pounds)
- cap set in capitals (CAPITALS)
- sm cap or s.c. set in small capitals (SMALL CAPITALS)
- lc set in lowercase (lowercase)
- ital set in italic (*italic*)
- rom set in roman (roman)
- bf set in boldface (boldface)
- = or -/ or ⊘ or /|/ hyphen
- <sup>1</sup>/<sub>2</sub> or en or /|/ en dash (1965-72)
- <sup>1</sup>/<sub>4</sub> or em or /|/ em — or long — dash
- √ superscript or superior (3as in vr<sup>2</sup>)
- ^ subscript or inferior (2as in H<sub>2</sub>O)
- ⊘ or x centered ⊘ for a centered dot in p · q)
- ⌒ comma
- ⌒ apostrophe
- ⊙ period
- ⌒ or ;/ semicolon
- : or ⊙ colon
- ⌒ or ⌒ quotation marks
- (/) parentheses
- [/] brackets
- OK/? query to author: has this been set as intended?
- ⌒ or ⌒<sup>1</sup> push down a ~~work-up~~
- ⊙ turn over an inverted letter
- wf<sup>1</sup> wrong font; a character of the wrong size or esp. style

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